IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Canceled).

Claim 2 (Previously Presented): A SiC semiconductor device comprising:

a semiconductor substrate having a (11-20), (000-1) or (0001) surface of a hexagonal or rhombohedral system P-type silicon carbide region, or a (110) surface of a cubic system P-type silicon carbide region;

a gate insulation layer formed on the silicon carbide region;

an effective P-type gate electrode formed on the gate insulation layer;

an N-type impurity region having an impurity concentration sufficient to form a buried channel region in a semiconductor layer on a lower surface of the gate insulation layer;

a diffusion region formed in the semiconductor substrate; and

source and drain regions comprised of N-type impurity regions formed adjacent to the gate insulation layer and gate electrode,

wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not more than 1.0 for the (000-1) or (110) surface and is not less than 0.2 and not more than 0.5 for the (11-20) or (0001) surface, where the L_{bc} is a depth of the buried channel region adjacent to a boundary formed by the N-type impurity region and the P-type silicon carbide region, and the X_j is a depth of the source and drain regions.

Claim 3 (Original): A device according to claim 2, wherein the gate electrode is comprised of polycrystalline silicon in which boron or aluminum is diffused at a concentration within a range of from 1×10^{16} cm^{-3} to 1×10^{21} cm^{-3}.

Claim 4 (Original): A device according to claim 2, wherein the gate electrode includes a silicide layer of a refractory metal.

Claim 5 (Original): A device according to claim 4, wherein the refractory metal is tungsten, molybdenum or titanium.

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Claim 6 (Original): A device according to claim 2, wherein the gate electrode is formed of aluminum or an alloy that contains aluminum.

Claim 7 (Original): A device according to claim 2, wherein the buried channel region contains a diffusion nitrogen, phosphorus or arsenic at a maximum concentration that is from 5×10^{15} cm^{-3} to 1×10^{18} cm^{-3}.

Claim 8 (Previously Presented): A device according to claim 2, wherein the diffusion region has an impurity concentration that is not lower than a maximum impurity concentration of the impurity region used to form the buried channel region and not higher than an impurity concentration of the source or drain regions.

Claim 9 (Previously Presented): A device according to claim 7, wherein the diffusion region has an impurity concentration that is not lower than a maximum impurity concentration of the impurity region used to form the buried channel region and not higher than an impurity concentration of the source or drain regions.

Claim 10 (Previously Presented): A device according to claim 8, wherein the diffusion region comprises nitrogen, phosphorus, or arsenic at a maximum concentration that is from 5×10^{16} cm^{-3} to 1×10^{19} cm^{-3}.

Claim 11 (Previously Presented): A device according to claim 9, wherein the diffusion region comprises nitrogen, phosphorus, or arsenic at a maximum concentration that is from 5×10^{16} cm^{-3} to 1×10^{19} cm^{-3}.

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Claim 12 (Previously Presented): A device according to claim 7, wherein the diffusion region is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel region.

Claim 13 (Previously Presented): A device according to claim 10, wherein the diffusion region is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel region.

Claim 14 (Previously Presented): A device according to claim 11, wherein the diffusion region is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel formation region.

Claim 15 (Previously Presented): A device according to claim 13, wherein the diffusion region is a high-concentration P-type impurity diffusion region located adjacently

under the buried channel region that includes an aluminum or boron diffusion region having a maximum impurity concentration of 1 x 10^{17} cm^{-3} to 1 x 10^{19} cm^{-3}.

Claim 16 (Previously Presented): A device according to claim 14, wherein the diffusion region is a high-concentration P-type impurity diffusion region located adjacently under the buried channel region that includes an aluminum or boron diffusion region having a maximum impurity concentration of 1 x 10^{17} cm^{-3} to 1 x 10^{19} cm^{-3}.

Claim 17-23 (Canceled).

Claim 24 (Original): A device according to claim 2, having a lateral resurf or lateral DMOS type MOSFET structure.

Claim 25 (Original): A device according to claim 6, having a lateral resurf or lateral DMOS type MOSFET structure.

Claim 26 (Original): A device according to claim 7, having a lateral resurf or lateral DMOS type MOSFET structure.

Claim 27 (Original): A device according to claim 8, having a lateral resurf or lateral DMOS type MOSFET structure.

Claim 28 (Original): A device according to claim 9, having a lateral resurf or lateral DMOS type MOSFET structure.

Claim 29 (Original): A device according to claim 12, having a lateral resurf or lateral DMOS type MOSFET structure.

Claim 30 (Original): A device according to claim 15, having a lateral resurf or lateral DMOS type MOSFET structure.

Claim 31 (Original): A device according to claim 16, having a lateral resurf or lateral DMOS type MOSFET structure.

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Claim 32 (Canceled).

Claim 33 (Original): A device according to claim 8, having a DMOS type MOSFET structure.

Claim 34 (Original): A device according to claim 9, having a DMOS type MOSFET structure.

Claim 35 (Original): A device according to claim 12, having a DMOS type MOSFET structure.

Claim 36 (Original): A device according to claim 13, having a DMOS type MOSFET structure.

Claim 37 (Original): A device according to claim 14, having a DMOS type MOSFET structure.

Claim 38 (Previously Presented): A device according to claim 2, having a DMOS type MOSFET structure.

Claim 39 (Previously Presented): A device according to claim 24, wherein at least one of the source and drain is formed of metal or an alloy containing nickel.

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Claim 40 (Currently Amended): A device according to claim 26,wherein at least one of the source and drain is formed of [[metal]] nickel or an alloy containing nickel.

Claim 41 (Currently Amended): A device according to claim 38, wherein at least one of the source and drain is formed of [[metal]] nickel or an alloy containing nickel.

Claim 42 (Currently Amended): A device according to claim 15, wherein at least one of the source and drain is formed of [[metal]] nickel or an alloy containing nickel.

Claim 43 (New): A device according to claim 2, further comprising metal wires formed on at least one of the source region, the drain region, and the gate electrode,

wherein the metal wires comprise nickel.